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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/776,009	02/02/2001	Michael A. Vyvoda	SDP113US	7430

67558 7590 05/01/2012

Cooper Legal Group LLC
6505 Rockside Road
Suite 330
Independence, OH 44131

EXAMINER	
MAI, ANH D	

ART UNIT	PAPER NUMBER
2829	

NOTIFICATION DATE	DELIVERY MODE
05/01/2012	ELECTRONIC

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte MICHAEL A. VYVODA, JAMES M. CLEEVES, and SAMUEL V. DUNTON

Appeal 2010-001997
Application 09/776,009
Technology Center 2800

Before HOWARD B. BLANKENSHIP, THU A. DANG, and JAMES R. HUGHES, *Administrative Patent Judges*.

DANG, *Administrative Patent Judge*.

DECISION ON APPEAL

I. STATEMENT OF THE CASE

Appellants appeal under 35 U.S.C. § 134(a) from a Final Rejection of claims 63-66 and 68-70 (App. Br. 3). Claim 67 is cancelled (App. Br. 10). We have jurisdiction under 35 U.S.C. § 6(b).

We affirm.

A. INVENTION

Appellants' invention is directed to a wafer having regions of hydrophobic material (a semiconductor) and hydrophilic material (a dielectric) that are exposed at the surface of the wafer; wherein, the percentage of the total surface area of the wafer that is hydrophobic material is less than or equal to a predetermined percentage of the total surface area of the wafer (Abstract; Spec. ¶ [0018]).

B. ILLUSTRATIVE CLAIM

Claim 63 is exemplary:

63. A wafer having a surface, the surface comprising:

a plurality of elongated strips of polysilicon; and

a plurality of elongated strips of dielectric material, the strips of dielectric material alternating with the strips of polysilicon,

wherein the surface has been planarized by chemical mechanical planarization, and

wherein a first percentage of total wafer surface area that is polysilicon is less than or equal to 70 percent.

C. REJECTIONS

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

Wu	US 6,008,087	Dec. 28, 1999

Claims 63-66 and 68-70 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Wu.

Claims 63-66 and 68-70 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Wu.

II. ISSUE

The dispositive issue before us is whether the Examiner has erred in finding that Wu discloses a wafer surface "wherein a first percentage of total wafer *surface area that is polysilicon is less than or equal to 70 percent*" (claim 63, emphasis added).

III. FINDINGS OF FACT

The following Findings of Fact (FF) are shown by a preponderance of the evidence.

1. Wu discloses polysilicon wall spacers (strips)16 having a thickness to 200-3000A (Figs. 4-6; col. 3, ll. 50-55).

2. The opening 12 filled with two polysilicon wall spacers 16 and one dielectric strip 20 has a width ranging from 500 to 5000 A (Figs. 2, 4-6; col. 3, ll. 37-40).

3. A thick oxide layer 20 (representing dielectric strips) replaces the silicon nitride layer 6 having a width of 300-3000A (Figs. 3-6; col. 3, ll. 36-37).

IV. ANALYSIS

Claims 63-66 and 68-70 under 35 U.S.C. § 102(b)

Appellants contend that "[t]o assume the relative widths of the polysilicon strips 16 and oxide 20 (and from those relative widths to infer their relative percentage of total surface area) from a subjective estimate of their appearance in Fig. 6, for example, in the absence of an explicit teaching, is improper" (App. Br. 6). Appellants argue that "the percent surface area of Wu's wafer surface that is polysilicon … is unknown" (*id.*). Appellants assert that the Examiner's finding that "some combinations of the dimensions disclosed in Wu *could* yield a polysilicon percentage area of 70 percent or less … cannot be supported" (App. Br. 7).

Although the Examiner finds that "[i]n Fig. 6 of Wu, the polysilicon strips 16 and the dielectric material strips 20 appears to be approximately the same size" (Ans. 6), we agree with the Appellants that "'it is well established that patent drawings do not define the precise proportions of the elements and may not be relied on to show particular sizes if the specification is completely silent on the issue'" (App. Br. 6 (quoting *Hockerson-Halberstadt, Inc. v Avia Group Int'l*, 222 F.3d 951,956, (Fed. Cir. 2000))).

Wu's Figures 2, 4 (annotated), and 6 (annotated) are reproduced below:

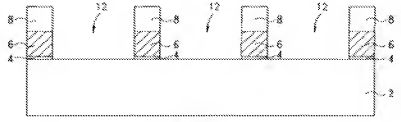

FIG.2

Figure 2 depicts a cross section view of a semiconductor wafer illustrating the step of etching the pad oxide and the silicon nitride layer (col. 2, ll. 48-50).

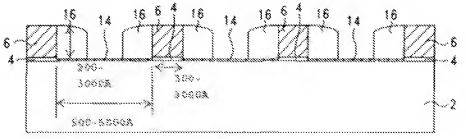

FIG.4

Annotated Figure 4 depicts a cross section view of the semiconductor wafer illustrating the step of forming polysilicon side wall spacers (col. 2, ll. 54-57).

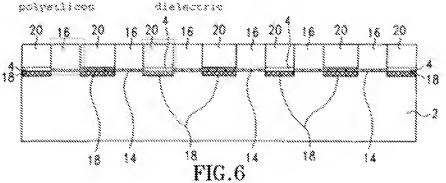

FIG.6

Annotated Figure 6 depicts a cross section view of the semiconductor wafer illustrating the steps of forming an oxide and performing chemical mechanical polishing (planarization) (col. 2, ll. 62-64).

As shown *supra* in Figure 2, the opening 12, having a width of 500 to 5000 angstroms, is filled with two polysilicon wall spacers 16 deposited next to a silicon nitride layer 6 as shown in Figure 4. Although the *thickness* of the polysilicon wall spacers 16 is disclosed as 200 to 3000 angstroms (FF 1), we note that the *width* of the polysilicon wall spacers 16 is not disclosed. Even though the width of the opening 12 including the at least two polysilicon wall spacers 16 and a thick oxide layer 20 (representing a dielectric strip) is disclosed to be within the range of 500 to 5000 angstroms (FF 2), we find that Wu is silent as to the surface area of polysilicon strips 16 being less than or equal to 70 percent of the total wafer surface area.

Our reviewing court held that "the disclosure of a range … does not constitute a specific disclosure of the endpoints of that range . . . . The disclosure is only that of a range, not a specific [measurement] in that range, and the disclosure of a range is no more a disclosure of the end points of the range than it is of each of the intermediate points." *Atofina v. Great Lakes Chemical Corp.*, 441 F.3d 991, 1000 (Fed. Cir. 2006).

Therefore, although the Examiner finds that "the dielectric materials 20, has a width of about 300 to 3000 angstroms" and "polysilicon strips 16 has a thickness or width of about 200 to 3000 angstroms," we do not agree that "one of ordinary skill in the art should reasonably conclude that the total surface area of polysilicon strips 16 is less than 70 percent of the total wafer surface area" (Ans. 6).

Accordingly, we find that Appellants have shown that the Examiner erred in rejecting independent claim 63 under 35 U.S.C. § 102(b) over Wu; and claims 64-66 and 68-70 depending from claim 63.

Claims 63-66 and 68-70 under 35 U.S.C. § 103(a)

Appellants provide arguments with respect to independent claim 63 (App. Br. 5-8). Appellants do not provide arguments with respect to dependent claims 64-66 and 68-70. Accordingly, we select claim 63 as being representative of the claims. *See* 37 C.F.R. § 41.37(c)(1)(vii).

Appellants repeat in the Reply Brief that the applied references fail to disclose a wafer surface "wherein a first percentage of total wafer surface area that is polysilicon is less than or equal to 70 percent" as recited in the claims (Reply Br. 3). Although Appellants additionally contend in the Reply Brief "[t]he surfaces are different in a way that is central to the invention, and this limitation is thus entitled to patentable weight" (Reply Br. 2), we note that this argument could have been raised in the Appeal Brief. That is, the Examiner's Answer contains the same findings as those set forth in the Final Rejection and, thus, does not necessitate this new argument by the Appellants. It is inappropriate for Appellants to discuss for the first time in the Reply Brief matters that could have been raised in the Appeal Brief. "The failure to raise all issues and arguments diligently, in a timely fashion, has consequences." *Ex parte Borden*, 93 USPQ2d 1473, 1475 (BPAI 2010) (informative decision). *Kaufman Company v. Lantech, Inc.*, 807 F.2d 970, 973 n.* (Fed. Cir. 1986).

As noted *supra*, Wu discloses a wafer having polysilicon strips and a thick oxide layer (representing dielectric strips) (FF 1 and 3); wherein, the dielectric strips that replace the silicon nitride layer 6 have a width of 300-3000A (FF3). Even though the dielectric strips that replace the thick oxide layer 20 have an undisclosed width, the opening including two polysilicon strips and the thick oxide layer has a width of 500 to 5000 A (FF 2). Hence,

according to the Appellants own admission, "[s]ome combinations of disclosed dimensions yield 70 percent polysilicon or less within the area shown in Fig. 6" (App. Br. 6).

Our reviewing Court has held that, in the case where the claimed ranges overlap or lie inside ranges disclosed by the prior art, a prima facie case of obviousness exists unless the applicant has shown that the particular range is critical ("by showing that the claimed range achieves unexpected results relative to the prior art range"). *In re Woodruff*, 919 F.2d 1575, 1578 (Fed. Cir. 1990). Here, Appellants have proffered no objective evidence of unexpected results when the surface area of polysilicon is 70 percent or less than the total surface area.

Therefore, we find that the Examiner has established the prima facie obviousness of the claims because Wu presents a prima facie case of obviousness for the claimed first percentage of the total wafer surface area that is polysilicon is less than or equal to 70 percent. As a result, we will sustain the Examiner's § 103 rejection of representative claim 63 and that of claims 64-66 and 68-70 depending from claim 63.

V. CONCLUSION AND DECISION

The Examiner's rejection of claims 63-66 and 68-70 under 35 U.S.C. § 102(b) is reversed, while the rejection of claims 63-66 and 68-70 under 35 U.S.C. § 103(a) is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

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